What is claimed is:

1. A method of fabricating a metal interconnect structure, on a semiconductor substrate, self-aligned to an underlying metal plug structure, comprising the steps of:

forming a lower level, metal interconnect structure;

depositing an interlevel dielectric, (ILD), layer;

forming a via hole in said ILD layer, exposing a portion of a top surface of said lower level, metal interconnect structure;

forming a recessed metal plug structure in a bottom portion of said via hole;

depositing a metal layer;

forming a photoresist shape on a portion of said metal layer, located on said ILD layer, and located in an inside edge of said via hole; and

patterning of said metal layer, using said photoresist shape as a mask, to form an upper level, metal interconnect structure comprised of: a metal structure component, defined from said portion of said metal layer protected by overlying said photoresist shape, and comprised of a metal ring component, not protected by said photoresist shape, during said patterning procedure, located in a top portion of said via hole, and with said metal ring component comprised of metal spacers on the sides of a top portion of said via hole, overlying and contacting a portion of said recessed metal plug structure.

2. The method of claim 1, wherein said lower level, metal interconnect structure is comprised of: an underlying titanium nitride layer, obtained via PVD procedures, at a thickness between about 100 to 1500 Angstroms, an aluminum, or aluminum - copper layer, obtained via PVD procedures, at a thickness between about 2000 to 20000 Angstroms; and an underlying titanium nitride layer, obtained via PVD procedures, at a thickness between about 100 to 1500 Angstroms.

3. The method of claim 1, wherein said ILD layer is a silicon oxide, or a borophosphosilicate glass layer, obtained via low pressure chemical vapor deposition, (LPCVD), or plasma enhanced chemical vapor deposition, (PECVD), procedures, at a thickness between about 5000 to 30000 Angstroms.

4. The method of claim 1, wherein said via hole is formed in said ILD layer via an anisotropic reactive ion etching, (RIE), procedure, using CHF_3 as an etchant.

5. The method of claim 1, wherein said via hole has a diameter between about 0.10 to 1.0 um.

6. The method of claim 1, wherein said recessed metal plug structure is a recessed tungsten plug structure, formed via deposition of a tungsten layer, via LPCVD procedures, at a thickness between about 2000 to 10000 Angstroms, and defined via a selective, anisotropic RIE procedure, using Cl_2 or SF_6 as an etchant.

7. The method of claim 1, wherein said recessed metal plug structure, in said bottom portion of said via hole, has a height between about 3000 to 20000 Angstroms.

8. The method of claim 1, wherein said metal layer is an aluminum, or an aluminum - copper layer, obtained via PVD procedures, at a thickness between about 2000 to 20000 Angstroms.

9. The method of claim 1, wherein said patterning procedure, used to form said upper level, metal interconnect structure, comprised of said metal structure component, and of attached, said metal ring component, is an anisotropic RIE procedure, applied to said metal layer, using Cl_2 or SF_6 an etchant.

10. A method of fabricating an upper level, metal interconnect structure, on a semiconductor substrate, with said upper level, metal interconnect structure self-aligned to an underlying, recessed tungsten plug structure, and with said upper level, metal interconnect structure comprised of a metal structure component, and an attached, metal ring component, with said metal ring component located in a top portion of a via hole, overlying and contacting said recessed tungsten plug structure, comprising the steps of:

forming a lower level, metal interconnect structure;

depositing an ILD layer;

forming a via hole in said ILD layer, exposing a portion of a top surface of said lower level, metal interconnect structure;

depositing a tungsten layer, completely filling said via hole;

performing a first anisotropic RIE procedure to remove regions of said tungsten layer from a top surface of said ILD layer, creating a tungsten plug structure in said via hole;

continuing said first anisotropic RIE procedure, to form said recessed tungsten plug structure, in a bottom portion of said via hole;

depositing a metal layer on the top surface of said ILD layer, and on said recessed tungsten plug structure, in said via hole;

forming a photoresist shape overlying a portion of said metal layer that is located on a portion of the top surface of said ILD layer, and overlying a portion of said metal layer that is located on edges of said recessed tungsten plug structure; and

performing a second anisotropic RIE procedure to remove regions of said metal layer, not protected by said photoresist shape, from the top surface of said ILD layer, creating said metal structure component, of said upper level, metal interconnect structure, while forming metal spacers on the sides of a top portion of said via hole, in regions unprotected by said photoresist shape, resulting in said metal ring component, of said upper level, metal interconnect structure, in said top portion of said via hole, with said metal ring component attached to said metal structure component, overlying and contacting said recessed tungsten plug structure, located in said bottom portion of said via hole.

11. The method of claim 10, wherein said lower level, metal interconnect structure is comprised of: an underlying titanium nitride layer, obtained via PVD procedures, at a thickness between about 100 to 1500 Angstroms, an aluminum, or aluminum - copper layer, obtained via PVD procedures, at a thickness between about 2000 to 20000 Angstroms; and an underlying titanium nitride layer, obtained via PVD procedures, at a thickness between about 100 to 1500 Angstroms.

12.The method of claim 10, wherein said ILD layer is a silicon oxide, or a borophosphosilicate glass layer, obtained via low pressure chemical vapor deposition, (LPCVD), or plasma enhanced chemical vapor deposition, (PECVD), procedures, at a thickness between about 5000 to 30000 Angstroms.

13. The method of claim 10, wherein said via hole is formed in said ILD layer via an anisotropic reactive ion etching, (RIE), procedure, using CHF_3 as an etchant.

14. The method of claim 10, wherein said via hole has a diameter between about 0.10 to 1.0 um.

15. The method of claim 10, wherein said tungsten layer is obtained via LPCVD procedures, at a thickness between about 2000 to 10000 Angstroms, using tungsten hexafluoride as a source.

16. The method of claim 10, wherein said first anisotropic RIE procedure, used to form said tungsten plug structure, in said via hole, and used to from said recessed tungsten plug structure, in said bottom portion of said via hole, is performed using Cl_2 or SF_6 as an etchant.

17.The method of claim 10, wherein said recessed tungsten plug structure, in said bottom portion of said via hole, has a height between about 3000 to 20000 Angstroms.

18. The method of claim 10, wherein said metal layer is an aluminum, or an aluminum - copper layer, obtained via PVD procedures, at a thickness between about 2000 to 20000 Angstroms.

19. The method of claim 10, wherein said second anisotropic RIE procedure, used to form said upper level, metal interconnect structure, comprised of said metal structure component, and of attached, said metal ring component, is performed using Cl_2 or SF_6 an etchant.

20. An upper level, metal interconnect structure, on a semiconductor substrate, comprising:

a lower level, metal interconnect structure;

an insulator layer on said lower level, metal interconnect structure;

a via hole in said insulator layer exposing a portion of a top surface of said lower level, metal interconnect structure;

a recessed metal plug structure, located in a bottom portion of said via hole, with said recessed metal plug structure overlying and contacting the portion of said lower level, metal interconnect structure, exposed in said via hole; and

said upper level, metal interconnect structure, comprised of a metal structure component, and of a metal ring component, with said metal structure component located on a portion of a top surface of said insulator layer, and also located on an edge of underlying, said recessed metal plug structure, and with said metal ring structure, attached to said metal structure component, located overlying, and contacting portions of a top surface of said recessed metal plug structure, with said metal ring component comprised of metal spacers on the sides of a top portion of said via hole.

21. The upper level, metal interconnect structure of claim 20, wherein said lower level, metal interconnect structure is comprised of a composite metal structure, featuring an aluminum, or an aluminum based layer, at a thickness between about 2000 to 20000 Angstroms, with an underlying titanium nitride layer, at a thickness between about 100 to 1500 Angstroms, and an overlying titanium nitride layer, at a thickness between about 100 to 1500 Angstroms.

22. The upper level, metal interconnect structure of claim 20, wherein said via hole is comprised with a diameter between about 0.10 to 1.0 um.

23. The upper level, metal interconnect structure of claim 20, wherein said recessed metal plug structure, is comprised of tungsten, with the height of said recessed metal plug structure, located in said bottom portion of said via hole, between about 3000 to 20000 Angstroms.

24. The upper level, metal interconnect structure of claim 20, wherein said metal ring structure, attached to said metal structure component of said upper level, metal interconnect structure, is comprised of aluminum, or aluminum - copper spacers, located on the sides of said top portion of said via hole.